



UNITED STATES PATENT AND TRADEMARK OFFICE

UNITED STATES DEPARTMENT OF COMMERCE
United States Patent and Trademark Office
Address: COMMISSIONER FOR PATENTS
P.O. Box 1450
Alexandria, Virginia 22313-1450
www.uspto.gov

| APPLICATION NO. | FILING DATE | FIRST NAMED INVENTOR | ATTORNEY DOCKET NO. | CONFIRMATION NO. |
|---|-------------|----------------------|---------------------|------------------|
| 09/801,913 | 03/09/2001 | Kesatoshi Takeuchi | 204155US2 | 2612 |
| 22850 | 7590 | 02/26/2004 | EXAMINER | |
| OBLON, SPIVAK, MCCLELLAND, MAIER & NEUSTADT, P.C. 1940 DUKE STREET ALEXANDRIA, VA 22314 | | | WANG, JIN CHENG | |
| | | ART UNIT | | PAPER NUMBER |
| | | 2672 | | 16 |
| DATE MAILED: 02/26/2004 | | | | |

Please find below and/or attached an Office communication concerning this application or proceeding.

| | | |
|------------------------------|------------------------|-----------------------------|
| Office Action Summary | Application No. | Applicant(s) |
| | 09/801,913 | TAKEUCHI ET AL. <i>S</i> |
| | Examiner | Art Unit |
| | Jin-Cheng Wang | 2672 |

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) Responsive to communication(s) filed on 30 January 2004.
 2a) This action is FINAL. 2b) This action is non-final.
 3) Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) Claim(s) 1-27 is/are pending in the application.
 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
 5) Claim(s) _____ is/are allowed.
 6) Claim(s) 1-27 is/are rejected.
 7) Claim(s) _____ is/are objected to.
 8) Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) The specification is objected to by the Examiner.
 10) The drawing(s) filed on _____ is/are: a) accepted or b) objected to by the Examiner.
 Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
 Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
 11) The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
 a) All b) Some * c) None of:
 1. Certified copies of the priority documents have been received.
 2. Certified copies of the priority documents have been received in Application No. _____.
 3. Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|--|---|
| 1) <input type="checkbox"/> Notice of References Cited (PTO-892) | 4) <input type="checkbox"/> Interview Summary (PTO-413) |
| 2) <input type="checkbox"/> Notice of Draftsperson's Patent Drawing Review (PTO-948) | Paper No(s)/Mail Date. _____ |
| 3) <input type="checkbox"/> Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____ | 5) <input type="checkbox"/> Notice of Informal Patent Application (PTO-152) |
| | 6) <input type="checkbox"/> Other: _____ |

DETAILED ACTION

Response to Amendment

1. The amendment filed on 1/30/2004 has been entered. Claims 1, 6, 11, 16, and 20 have been amended. Claims 24-27 have been newly added.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1-4, 6-9, 11-14, and 16-23 are rejected under 35 U.S.C. 102(e) as being anticipated by Odryna et al. U.S. Pat. No. 6,333,750 (hereinafter Odryna).

4. Claim 1:

Odryna teaches an overlay image processing device for generating an overlay image signal composed of an n number of superimposed image signals, n being an integer greater than 2, the overlay image processing device comprising:

A plurality of digital decoders configured to digitally decode a plurality of image signals (e.g., the decoder in Figure 21 and the Input A or Input B of Figure 17 incorporating Figure 21 constitute a plurality of digital decoders for the device of Figure 17);

An image selector (e.g., system 110) configured to receive outputs from each of the plurality of digital decoders (the Input A or Input B of Figure 17 incorporating Figure 21 constitute a plurality of digital decoders for the device of Figure 17) and configured to select from among a plurality of digitally decoded image signals one reference image signal and (n-1) number of superimposing image signals (See, column 15-25);

A plurality of resolution converters (scaler 184 of Figure 21) constitutes a resolution converter and the device of Figure 17 incorporating a plurality of overlay cards 180 of Figure 21 incorporates a plurality of resolution converters) configured to receive respective outputs directly from the image selector (e.g., system card 110 controlling the control gate array 188 etc.), such that each resolution converter can input any of the respective outputs, to convert resolutions of the n number of selected image signals into respective desired resolutions (column 20), and to output the converted image signals to an image synthesizer (the pixel bus 114 constitutes an image synthesizer performing overlaying operation on a pixel-by-pixel basis; see for example, column 20, lines 15-20; column 15, lines 58-67; column 16, lines 1-15), wherein the image synthesizer is configured to superimpose the (n-1) number of converted superimposing image signals on the converted one (1) reference signal (e.g., column 20, lines 15-20; column 15, lines 58-67; column 16, lines 1-15).

Claim 2:

The claim 2 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of at least one of the plurality of image signals being a display signal output from a personal computer. However, Odryna further discloses the claimed limitation of at least

one of the plurality of image signals being a display signal output from a personal computer (e.g., column 18).

Claim 3:

The claim 3 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the image selector selects the reference image signal and the (n-1) number of superimposing image signals according to an arbitrary predetermined order of superposition for the n number of image signals; and the image synthesizer superimposes the (n-1) number of converted superimposing image signals on the converted reference image signal according to the order of superposition.

However, Odryna further discloses the claimed limitation of the image selector selects the reference image signal and the (n-1) number of superimposing image signals according to an arbitrary predetermined order of superposition for the n number of image signals; and the image synthesizer superimposes the (n-1) number of converted superimposing image signals on the converted reference image signal according to the order of superposition (e.g., figures 17-21; column 15-25).

Claim 4:

The claim 4 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of a scan converter configured to convert at least one of the interlaced image signals selected by the image selector into a non-interfaced image signals selected by the image selector into a non-interlaced image signal when the at least one of the image signals selected by the image selector is an interlaced image signal.

However, Odryna further discloses the claimed limitation of a scan converter configured to convert at least one of the interlaced image signals selected by the image selector into a non-interfaced image signals selected by the image selector into a non-interlaced image signal when the at least one of the image signals selected by the image selector is an interlaced image signal (e.g., figures 17-21; column 15-25).

5. Claim 6:

Odryna teaches an overlay image display device for displaying an overlay image composed of an number of superimposed images, n being an integer greater than 1, the overlay image display device comprising:

An overlay image processing device (figure 17) for generating an overlay image signal composed of an n number of superimposed image signals, and the overlay display device for displaying an image represented by the overlay image signal; wherein the overlay image processing device (e.g., figure 17-21; column 15-25) includes:

A plurality of digital decoders configured to digitally decode a plurality of image signals (e.g., the decoder in Figure 21 and the Input A or Input B of Figure 17 incorporating Figure 21 constitute a plurality of digital decoders for the device of Figure 17);

An image selector (e.g., system 110) configured to receive outputs from each of the plurality of digital decoders (the Input A or Input B of Figure 17 incorporating Figure 21 constitute a plurality of digital decoders for the device of Figure 17) and configured to select

from among a plurality of digitally decoded image signals one reference image signal and (n-1) number of superimposing image signals (See, column 15-25);

A plurality of resolution converters (scaler 184 of Figure 21) constitutes a resolution converter and the device of Figure 17 incorporating a plurality of overlay cards 180 of Figure 21 incorporates a plurality of resolution converters) configured to receive respective outputs directly from the image selector (e.g., system card 110 controlling the control gate array 188 etc.), such that each resolution converter can input any of the respective outputs, to convert resolutions of the n number of selected image signals into respective desired resolutions (column 20), and to output the converted image signals to an image synthesizer (the pixel bus 114 constitutes an image synthesizer performing overlaying operation on a pixel-by-pixel basis; see for example, column 20, lines 15-20; column 15, lines 58-67; column 16, lines 1-15), wherein the image synthesizer is configured to superimpose the (n-1) number of converted superimposing image signals on the converted one (1) reference signal (e.g., column 20, lines 15-20; column 15, lines 58-67; column 16, lines 1-15).

Claim 7:

The claim 7 encompasses the same scope of invention as that of claim 6 except additional claimed limitation of at least one of the plurality of image signals being a display signal output from a personal computer. However, Odryna further discloses the claimed limitation of at least one of the plurality of image signals being a display signal output from a personal computer (e.g., column 18).

Claim 8:

The claim 8 encompasses the same scope of invention as that of claim 6 except additional claimed limitation of the image selector selects the reference image signal and the (n-1) number of superimposing image signals according to an arbitrary predetermined order of superposition for the n number of image signals; and the image synthesizer superimposes the (n-1) number of converted superimposing image signals on the converted reference image signal according to the order of superposition. However, Odryna further discloses the claimed limitation of the image selector selects the reference image signal and the (n-1) number of superimposing image signals according to an arbitrary predetermined order of superposition for the n number of image signals; and the image synthesizer superimposes the (n-1) number of converted superimposing image signals on the converted reference image signal according to the order of superposition (figures 17-21; column 15-25).

Claim 9:

The claim 9 encompasses the same scope of invention as that of claim 6 except additional claimed limitation identical to that set forth in claim 4. The claim 9 is rejected for the same reason set forth in claim 4.

6. Claims 11-14:

Each of the claims 11-14 is a rephrasing of the claims 1-4 respectively in a method form. The claims are rejected for the same reason as set forth above.

7. Claims 16-19:

Each of the claims 16-19 encompasses the same scope of invention as that of claims 1-4.

The claims are subject to the same rationale of rejection set forth in claims 1-4.

8. Claims 20-23:

Each of the claims 20-23 is a rephrasing of the claims 16-19 respectively in a method form. The claims are rejected for the same reason as set forth above.

Claim Rejections - 35 USC § 103

9. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

10. Claims 5,10, and 15 are rejected under 35 U.S.C. 103(a) as being unpatentable over Odryna et al. U.S. Pat. No. 6,333,750 (hereinafter Odryna) in view of Glen U.S. Patent No. 6,157,415 (Glen).

Claim 5:

(1) The claim 5 encompasses the same scope of invention as that of claim 1 except additional claimed limitation of the image synthesizer having the n number of 2-input image synthesizers, each 2-input image synthesizer being configured to receive upper-side and lower-side image signals and superimpose the upper-side image signal on the lower-side image signal; the n number of 2-input image synthesizers being connected in series in multistage fashion such that the 2-input image synthesizer of a first stage uses the reference image signal as the lower-

Art Unit: 2672

side image signal and a first superimposing image signal as the upper-side image signal, while the 2-input image synthesizer of ith stage, where I is between 2 and n, inclusive, uses an output of the 2-input image synthesizer of (I - 1)th stage as the lower-side image signal and ith superimposing image signal as the upper-side image signal.

(2) Odryna teaches the limitation set forth in the claim 1. However, Odryna lacks a full disclosure of the claim limitation.

(3) However, Glen further discloses the claimed limitation of the image synthesizer having the n number of 2-input image synthesizers, each 2-input image synthesizer being configured to receive upper-side and lower-side image signals and superimpose the upper-side image signal on the lower-side image signal; the n number of 2-input image synthesizers being connected in series in multistage fashion such that the 2-input image synthesizer of a first stage uses the reference image signal as the lower-side image signal and a first superimposing image signal as the upper-side image signal, while the 2-input image synthesizer of ith stage, where I is between 2 and n, inclusive, uses an output of the 2-input image synthesizer of (I - 1)th stage as the lower-side image signal and ith superimposing image signal as the upper-side image signal (Glen figures 5, 6 and 9, and column 3, lines 51-65).

(4) It would have been obvious to one of ordinary skill in the art to have incorporated the Glen's image synthesizer into the Odryna's overlay image processing device because Odryna suggests overlaying data can be merged into the base image on the pixel bus 114 on a pixel-by-pixel basis or according to various algorithms pre-programmed into the local control gate array and therefore suggesting the overlay steps can be controlled in a multistage fashion according to the overlay window (Odryna column 20-21; column 15-16).

Art Unit: 2672

(5) One having the ordinary skill in the art would have been motivated to do this because it would have provided a multistage synthesis for overlaying the portions of the input images (Glen column 3-4).

Claim 10:

The claim 10 encompasses the same scope of invention as that of claim 6 except additional claimed limitation identical to that set forth in claim 5. The claim 10 is rejected for the same reason set forth in claim 5.

Claim 15:

The claim 15 is a rephrasing of the claim 5 respectively in a method form. The claims are rejected for the same reason as set forth above.

11. Claims 24-27 are rejected under 35 U.S.C. 103(a) as being unpatentable over Odryna et al. U.S. Pat. No. 6,333,750 (hereinafter Odryna).

Claim 24-25:

(1) The claim 24 encompasses the same scope of invention as that of claim 6 except additional claimed limitation of the respective outputs of the image selector include an analog RGB signal and a horizontal sync signal, wherein each of the resolution converters generates a clock signal synchronized with the horizontal sync signal and corresponding to a pixel clock for the analog RGB signal, and quantizes the RGB signal in synchronism with the clock signal to

Art Unit: 2672

convert the analog RGB signal to a digital RGB signal, and wherein a single image signal element quantized by each of the resolution converters corresponds to one pixel of the image represented by the RGB signal.

(2) Odryna teaches the limitation set forth in the claim 6. However, Odryna's teaching of the resolution converter is configured by separating functionality of image decoding and resolution converting.

(3) Odryna teaches the image decoder for converting analog RGB signal to a digital RGB signal wherein the image decoder and the scaler of Figure 21 meets the claim limitation recited in claim 24.

(4) It would have been obvious to one of ordinary skill in the art to have moved some functionality from the image decoder into the resolution converter of Odryna because the circuits of the image decoder can be reconfigured and therefore by incorporating some of the reconfigured circuits into the scaler of Figure 21 of Odryna a new resolution converter can be constructed.

(5) One having the ordinary skill in the art would have been motivated to do this because it would have provided a resolution converter with additional functionalities.

Claim 25:

The claim 25 is subject to the same rationale of rejection set forth in the claim 24.

Claim 26:

The claim 26 is subject to the same rationale of rejection set forth in the claim 24.

Claim 27:

The claim 27 is subject to the same rationale of rejection set forth in the claim 24.

Art Unit: 2672

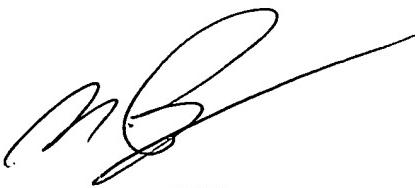
Conclusion

12. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Jin-Cheng Wang whose telephone number is (703) 605-1213. The examiner can normally be reached on 8:00 AM - 4:30 PM.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mike Razavi can be reached on (703) 305-4713. The fax phone numbers for the organization where this application or proceeding is assigned are (703) 308-6606 for regular communications and (703) 308-6606 for After Final communications.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist whose telephone number is (703) 395-3900.

jcw
February 17, 2004



MICHAEL RAZAVI
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2600